#9/Appeal Brief 6/26/02 Anne Th

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:		Docket No.:	TI-31026
	Jonathan Brodsky, et al.	Art Unit:	2814
Serial No.:	09/668,999	Examiner:	Dana Farahani
Filed:	September 25, 2000	Date:	June 11, 2002

Confirmation No.: 3740

For: CIRCUIT AND METHOD FOR AN INTEGRATED CHARGED DEVICE MODEL CLAMP

Assistant Commissioner for
Patents
Washington, D.C. 20231

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)

I hereby certify that on 6-11-02, this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231.

Ann Trent
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APPEAL BRIEF PURSUANT TO 37 C.F.R. § 1.192

Dear Sir:

Further to the Notice of Appeal mailed on even date, June 11, 2002, (Paper No. 6), this is Appellants' Appeal Brief, hereby submitted in triplicate in compliance with 37 C.F.R. § 1.192.

Real Party in Interest under 36 C.F.R. §1.191(c)(1)

The real party in interest in this application is Texas Instruments Incorporated, a corporation of the State of Delaware.

Related Appeals and Interferences under 36 C.F.R. §1.191(c)(2)

There are none.

Status of Claims:

Claims 1 - 24 are rejected

The claims on appeal are Claims 1 - 24.

Status of Amendments:

No amendment was submitted after the Final Office Action.

Summary of Invention:

The invention is an integrated electronic circuit providing improved electrostatic discharge ("ESD") protection. As is known in the art, as the numerous electronic devices that make up an integrated circuit have become ever smaller, allowing ever more of such devices to be placed on a single integrated circuit chip, the devices have also become ever more susceptible to ESD damage.

ESD events can arise from a number of different circumstances, but typically occur when an IC is handled by a human being or a machine. Charge accumulated on the device is suddenly discharged when contact is made between, for example, an input/output ("I/O") pin and an object that is grounded, called a charged device model ("CDM") event. Other types of ESD events can occur. In any event, this sudden discharge of the accumulated charge gives rise to a very brief, but high magnitude current. This ESD current most commonly causes damage to an IC by rupturing the thin dielectrics in the IC, such as metal oxide semiconductor ("MOS") gate oxides or capacitor dielectrics.

To avoid such damage, clamps have been used in the prior art to limit the voltage to which the thin dielectrics are subjected by the flow of the ESD current, and thereby prevent their rupture. These clamps are frequently called CDM clamps. However, generally in such prior art circuits, the clamp devices are separated from the internal input circuit transistors with a metal interconnect system providing the electrical connections between the clamps and the input circuit.

This metal interconnect system can significantly increase the parasitic resistance and inductance of the circuit. Thus, the parasitic inductance and resistance between the ground connection of the clamp and ground connection of the input circuit act in series with the clamp voltage of the clamp, building up excess voltage across the pin being protected and ground. Likewise, the parasitic inductance and resistance between the power-supply connection of the

clamp and the power-supply connection of the input circuit act in series with the clamp voltage of the clamp, building up excess voltage. Because a CDM type ESD event may have a peak current level of approximately 5 to 10 amps, with a rise time of only a few hundred picoseconds, the voltage drop along the ground/power-supply bus metallization may be significant with respect to the CDM clamp voltage. The total voltage drop may be high enough to degrade or even rupture the gate oxides of the input transistors.

The present invention generally overcomes these problems. The way in which these problems are overcome is by the placement of the CDM clamp circuit and the interface circuit adjacent to each other and by having them share a common device element. For example, the CDM clamp circuit that is integrated into the integrated circuit that it is protecting may share the same silicon source region. Other device elements could be shared, for example drains, by having the two devices share the same silicon drain region in the integrated circuit.

An example of this adjacent CDM clamp circuit and interface circuit sharing a common device element is shown in Figure 4C of the instant Application, which is a cross-sectional view of an embodiment of the present invention that is an IC input circuit with integrated CDM clamps. A circuit diagram of the IC shown in Figure 4C is shown in Figure 4A. Devices 416 and 418 (Figure 4A) comprise the CDM clamp circuit, while devices 412 and 414 comprise the interface circuit. In Figure 4C it can be seen that CDM clamp device 416, comprising source 430, gate 428 and drain 426, and interface circuit device 412, comprising source 430, gate 432 and drain 434, share a common source, namely source 430. Likewise, CDM clamp device 418, comprising source 440, gate 442 and drain 444, and interface circuit device 414, comprising source 440, gate 438 and drain 436, share a common source, namely source 440. This circuit is described in detail in the instant Specification, at page 8, line 12, et seq.

The inventive technique of placing of the CDM clamp circuit and the interface circuit adjacent to each other and having them share a common device element eliminates the need for a metal interconnect between the common device element, thus minimizing, or even eliminating parasitic resistance and inductance between the ground/power-supply connection of the internal input circuitry and the ground/power-supply connection of the CDM clamp device, thereby preventing the rupture of the thin dielectrics in the IC from ESD events.

A further advantage of the present invention is that by locating the devices adjacent to one another and having them share a common device element, the area needed on the integrated circuit for CDM protection is reduced.

Issues:

There are two issues on appeal:

1. Whether Claims 1 – 17 and 21 are unpatentable under 35 U.S.C. 102(e) as being anticipated by Pan (U.S. Patent No. 6,281,554 B1).

2. Whether claims 18, 22, 19 – 20 and 23 – 24 are unpatentable under 35 U.S.C. 103(a) over Pan, as applied to Claims 17 and 21, and further in view of Utsunomiya et al. (U.S. Patent No. 6,207,996 B1).

Grouping of Claims:

There are two groups of claims, Group I comprising Claims 1 - 16, and Group II comprising Claims 17 - 24, for the reasons set forth immediately below.

Group I. Independent Claim 1 recites an integrated circuit comprising an I/O pad, an interface circuit connected to the I/O pad, and a CDM clamp circuit connected to the pad and to the interface circuit, wherein the CDM clamp circuit and the interface circuit "are adjacent to each other and share a common device element." Claim 10, the only other independent claim in Group I, recites a method of protecting an integrated circuit from ESD, the integrated circuit comprising an I/O pad and an interface circuit connected to the I/O pad, the method comprising the steps of disposing a CDM clamp circuit "adjacent to said interface circuit" and connected to the pad and to the interface circuit, and "sharing a common device element between both said CDM clamp circuit and said interface circuit." Thus, both independent claims in Group I recite the limitations that the CDM clamp circuit and the interface circuit are adjacent to each other and share a common device element.

Group II. Independent Claim 17 recites an integrated circuit comprising (1) a semiconductor substrate; (2) a first drain region in the substrate, a first channel region in the substrate directly adjacent to the first drain region, a first gate dielectric overlying the first channel region, a first gate overlying the first gate dielectric, and a first source region disposed in

the substrate *directly adjacent to the first channel region*; and (3) a second channel region disposed in the substrate *directly adjacent to the first source region and on a side of the first source region opposite to the first channel region*, a second gate dielectric overlying the second channel region, a second gate overlying the second gate dielectric, and a second drain region disposed in the substrate directly adjacent to the second channel region. Claim 21, the only other independent claim in Group II, similarly recites a method of forming an integrated circuit comprising the steps of (1) forming a first drain region in a semiconductor substrate, forming a first source region in the substrate *separated from the first drain region solely by a first channel region*; (2) forming a second drain region in the substrate *separated from the first source region solely by a second channel region, wherein the second channel region is a different region than the first channel region*; and (3) forming a first gate dielectric overlying the first channel region and a second dielectric overlying the second channel region, and forming a first gate overlying the first gate dielectric and a second gate overlying the second gate dielectric. Thus, in both Claim 17 and Claim 21 two distinct semiconductor devices are recited that are adjacent to one another, in Claim 17 the recitation being of an apparatus, i.e., the two devices themselves, while in Claim 21 the recitation being of a method of forming such an apparatus, while both claims recite a single source region that, as so recited is shared by the two devices, i.e., both devices use the same source region.

The difference of Group II from Group I is that the Group II claims do not use the word "share" to describe the relation of the common source region to the respective adjacent devices, and, while it is clear from the recitation of elements in Claim 21 that the two devices are adjacent to one another (see, especially, the emphasized text), the word "adjacent" is not used to describe their respective relation to one another in that claim. However, conceptually Groups I and II recite two devices adjacent to one another and sharing a common device element, specifically, a source region in the Group II claims. They are called out as distinct groups because of the language difference between them, which slightly impacts the Argument, hereinbelow, and which might be seen as reason to treat the two groups differently.

Argument:

The argument is provided in three subsections, since there are two groups of claims, and the two issues are split between the two groups:

Subsection 1 argues that the patent to Pan does not teach or suggest an integrated circuit having a CDM clamp circuit and an interface circuit that are adjacent to one another and that share a common device element. This argues for the allowability of Claims 1 – 16 in the first issue, Claims 1 – 16 being all of the Group I claims.

Subsection 2 argues that the patent to Pan does not teach nor suggest an integrated circuit having two devices that are adjacent to one another and that share a common source. This argues for the allowability of Claims 17 and 21, the remaining claims in the first issue, Claims 17 and 21 being the only two independent claims in Group II.

Subsection 3 argues that the patent to Utsunomiya et al. does not cure the deficiencies of Pan. Thus, the patent to Utsunomiya et al. does not teach nor suggest an integrated circuit having two devices that are adjacent to one another and that share a common source region. This argues for the allowability of Claims 18, 22, 19 – 20 and 23 – 24, all of the claims in the second issue, and all being members of the Group II claims.

1. The patent to Pan does not teach nor suggest an integrated circuit having a CDM clamp circuit and an interface circuit that are adjacent to one another and that share a common device element, as required by Claims 1 – 16.

The patent to Pan discloses an ESD discharge protection circuit of the type described above in the "Summary of Invention" section that represents the prior art approach. The problem addressed by Pan can be understood by referring to Figures 1 and 2 of Pan, Figure 2 providing a schematic diagram of an ESD protection circuit comprising devices 16 and 42 for an input circuit comprising the two unnumbered devices to the right of the figure, and with Figure 1 showing a cross-sectional view of the actual structure of devices 16 and 42 of Figure 2. Due to the requirements of the high-voltage fabrication process used to make devices 16 and 42, the P-well region 14 shown in Figure 1 is formed with high resistance. Consequently, two parasitic bipolar junction transistors, shown as 66 and 68 in Figure 1, have a higher breakdown voltage. However, as shown in Figure 2, the gates of the PMOS transistor 16 and the NMOS transistor 42 are electrically connected to V_{DD} and V_{SS}. As a result, it is difficult to turn on the parasitic bipolar transistors 66 and 68 in a short time, so as to be able to conduct ESD current and thereby protect the input circuit.

To solve the problem, Pan proposes providing adding parasitic capacitors to allow rapid turn-on of the parasitic bipolar transistors. These capacitors are shown in Figure 4 as blocks 148 and 150. Pan claims that in Figure 3 these capacitors are shown as formed under the polysilicon "gate" region 128. See Pan, column 3, lines 53 – 58. However, even if one were to regard devices 132/146 and 110/144 as a clamp circuit, and Pan does not say it is one, it is clear that Pan neither shows nor suggests that either such device shares a common element with the interface circuit represented by the unnumbered devices to the right of Figure 4. In fact, Pan does not even show those unnumbered devices in the cross-sectional view of his apparatus in Figure 3. This shows clearly that Pan is unconcerned with the devices 132/146 and 110/144 being adjacent to the unnumbered devices comprising his interface circuit. It follows perforce that they share no common device element.

In the Final Office Action in the instant application, dated May 29, 2002, it was stated at page 2 thereof with respect to Pan that "The charge device model claim circuit [i.e., 144 and 146] and the interface circuit [i.e., at the right end of Figure 4] are adjacent to each other and share a common device element by a V_{DD} line at the top of the figure." Apparently by way of attempting to explain this illogical statement, the Final Office Action goes on to state at page 6 thereof, that "the applicant [sic] argues that the ESD protection device and the interface circuit in Pan reference do not share a common device element, and the two are not adjacent to each other. This is not found persuasive since, although not shown in figure 3, but as can be seen in figure 4, the ESD protection device and the interface circuit share a source region and they are adjacent to each other." Thus, the argument is that because figure 4 of Pan shows the sources of two devices are connected to V_{DD} Pan thus teaches that they share a common source region.

Applicants respectfully assert that this argument from the Final Office Action presents a gross misconstruction of clear claim language, representing a baseless attempt at reconstruction of the claimed invention with the benefit of hindsight. The argument against patentability clearly hinges on the concepts of "adjacent" and "sharing" a "common" device element. Regarding adjacency, the Examiner concedes that no adjacency of the ESD protection device and the interface circuit is shown in Figure 3 of Pan, which is the cross-sectional view that actually shows the devices. Instead, the Examiner attempts to establish adjacency by way of Figure 4, which is only a circuit diagram, having no necessary bearing on where the actual

devices may be formed in the integrated circuit, other than that they will be electrically interconnected as represented in the circuit diagram. Thus, no teaching or suggestion of adjacency can be inferred from the circuit diagram, as the Examiner attempts to do. The attempt to do so reveals an attempt to reconstruct the invention with the benefit of hindsight, since the Examiner knows what the instant Specification teaches, and what the Claims in issue recite.

Regarding the sharing of a common device element, the concept is so notoriously well known and frequently used that reference to a dictionary would seem to be superfluous, especially since the usage throughout the instant Specification is consistent with such notoriously well known usage. For example, regarding its well known usage, who can say it is not understood that if twins are born "sharing a common heart" that they are Siamese twins having but a single heart? Does saying that twins are born "sharing a common heart" mean that there is one heart that both twins use and upon which both twins rely? Or, does it mean that they each have their own heart and those separate hearts are connected, say, by a vein that runs between them? Clearly, the latter interpretation is incorrect. But, that is exactly the interpretation the Examiner is inviting us to adopt.

The usage in the instant Specification and Claims is consistent with dictionary definitions. In Webster's Third New International Dictionary, © 1976, G. & C. Merriam Co., "share" is defined as, "to participate in, take, possess, or undergo in common." [2]share, def. 4. In that same reference, "common" is defined as "held, enjoyed, experienced, or participated in equally by a number of individuals: possessed or manifested by more than one individual." [1]common, def. 2a. These definitions are not consistent with the concept of two separate things connected by a third element. However, they are consistent with the usage adopted in the instant Specification and Claims, and upon which patentability of at least the Group I claims rests. Note that the Group II claims do not require interpretation of these terms, as the element/step recitation establishes such relationships by the manner of their recitation.

Finally, it is well settled law that claims are to be interpreted in light of the specification. Thus, it is appropriate to read the specification to determine whether the use of these terms is consistent with their commonly understood meaning, or the meaning the Examiner invites us to give them. It is clear that such usage is consistent with their commonly understood meaning. For example, in the Specification, at page 9, lines 3 – 8, it states,

"As can be seen in Figs. 4B and 4C, PMOS input transistor 412 and CDM clamp PMOS transistor 416 *share* p+ source region 430 as a single source for both devices. Similarly, NMOS input transistor 414 and CDM clamp NMOS transistor 418 *share* n+ source region 440 as a single source for both devices. A metal interconnect layer is not needed to connect the source regions of the devices, thus avoiding the parasitic resistance and inductance created by the metal interconnect of prior art devices." (emphasis added.)

Looking at Figures 4B and 4C, we see that source region 430 is a single region shared by PMOS input transistor 412 and CDM clamp PMOS transistor 416, not two separate regions for each such transistor, connected by a metal interconnect. In fact, two source regions connected by a metal interconnect layer is explicitly stated as being what Figures 4B and 4C do NOT show.

Clearly, the interpretation set forth in the Final Office Action cannot stand. It has nothing on which to stand, and it flies in the face of the specification.

Therefore, it is respectfully submitted, Claims 1 – 16 are patentable over Pan, since the explicit limitation in independent Claims 1 and 10, namely, that they require a CDM clamp circuit and an interface circuit that are adjacent to each other and share a common device element, is neither shown nor suggested by Pan.

2. The patent to Pan does not teach nor suggest an integrated circuit having two devices that are adjacent to one another and that share a common source.

It was pointed out in the previous subsection under this Arguments section that, in Pan, even if one were to regard devices 132/146 and 110/144 as a clamp circuit, it is clear that Pan neither shows nor suggests that either such device is shares a common element, much less a common source, with the interface circuit represented by the unnumbered devices to the right of Figure 4. In fact, Pan shows no two devices that are adjacent to one another and that share a common source or any other device element, which is de facto what is recited in independent Claims 17 and 21, as described in detail above in the Summary of Invention section. Therefore, it is respectfully submitted that Claims 17 and 21 are patentable over Pan for that reason.

3. The patent to Utsunomiya et al. does not cure the deficiencies of Pan. Thus, the patent to Utsunomiya et al. does not teach nor suggest an integrated circuit having two devices that are adjacent to one another and that share a common source.

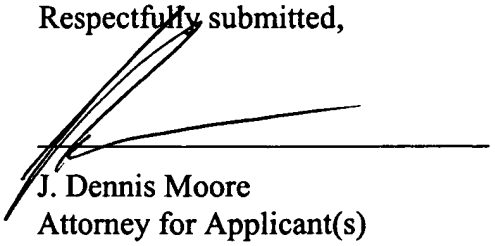
The patent to Utsunomiya et al. apparently relates to a semiconductor device and method for manufacturing a semiconductor device having a silicon on insulator ("SOI") structure and having an SOI static electricity protection circuit. There is no teaching or suggestion in the patent to Utsiunomiya et al. of any devices sharing any element, much less sharing a source region. For example, Figure 1 of Utsiunomiya et al. shows an internal circuit 102 formed by a MOSFET 105 and an SOI static electricity protection circuit 101 formed by an N-channel MOSFET 104. Figure 4 shows a MOSFET configured as an SOI static electricity protection circuit, such as MOSFET 104 of Figure 1. However, the drain 202 of this circuit is merely connected somehow to the I/O pad 103. The action of the circuit shown in Figure 1 protects the internal circuit "connected to the input output pad 103" (col. 5, lines 55-56). Clearly, the internal circuit and the device/circuit shown in Figure 4 do not share any device element, much less share a source region.

The allowability over Pan of independent Claims 17 and 21 of the Group II claims is argued in subsection (2), hereinabove. The remaining Group II Claims all depend, either directly or indirectly, from one of Claims 17 and 21. Therefore, it is respectfully submitted that Claims 18, 22, 19 – 20 and 23 – 24, all members of the Group II claims, are patentable over Pan and Utsunomiya et al. for the reasons set forth hereinabove.

Relief Requested:

For all of the reasons set forth hereinabove, allowance of Claims 1 - 24 is respectfully requested.

Respectfully submitted,



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Appendix 1
(Copy of Claims involved in the Appeal)

1. An integrated circuit comprising:

an input/output (I/O) pad;

an interface circuit connected to said I/O pad; and

a charged device model (CDM) clamp circuit connected to said pad and to said interface circuit, wherein said CDM clamp circuit and said interface circuit are adjacent to each other and share a common device element.

2. The integrated circuit of claim 1, further comprising a resistor disposed between said I/O pad and said interface circuit.

3. The integrated circuit of claim 1, wherein said CDM clamp circuit comprises a first transistor and said interface circuit comprises a second transistor.

4. The integrated circuit of claim 3, wherein said first and second transistors are MOS transistors.

5. The integrated circuit of claim 4, wherein said CDM clamp circuit and said interface circuit share a common source region.

6. The integrated circuit of claim 1, wherein said I/O pad is an input pad and said interface circuit is an input circuit.

7. The integrated circuit of claim 6, wherein said CDM clamp circuit comprises a first PMOS transistor and said interface circuit comprises a second PMOS transistor, and wherein said common device element is a p+ source region.

8. The integrated circuit of claim 6, wherein said CDM clamp circuit comprises a first NMOS transistor and said interface circuit comprises a second NMOS transistor, and wherein said common device element is an n+ source region.

9. The integrated circuit of claim 6, wherein said CDM clamp circuit comprises a first PMOS transistor and a first NMOS transistor, wherein said interface circuit comprises a second PMOS transistor and a second NMOS transistor, wherein said first and second PMOS transistors share a p+ source region, and wherein said first and second NMOS transistors share an n+ source region.

10. A method of protecting an integrated circuit from electrostatic discharge (ESD), said integrated circuit comprising an input/output (I/O) pad and an interface circuit connected to said I/O pad, said method comprising:

disposing a charged device model (CDM) clamp circuit adjacent to said interface circuit and connected to said pad and to said interface circuit; and

sharing a common device element between both said CDM clamp circuit and said interface circuit.

11. The method of claim 10, wherein said CDM clamp circuit comprises a first MOS transistor and said interface circuit comprises a second MOS transistor.

12. The method of claim 11, wherein said common device element is a source region.

13. The method of claim 10, wherein said I/O pad is an input pad and said interface circuit is an input circuit.

14. The method of claim 13, wherein said CDM clamp circuit comprises a first PMOS transistor and said interface circuit comprises a second PMOS transistor, and wherein said common device element is a p+ source region.

15. The method of claim 13, wherein said CDM clamp circuit comprises a first NMOS transistor and said interface circuit comprises a second NMOS transistor, and wherein said common device element is an n+ source region.

16. The method of claim 13, wherein said CDM clamp circuit comprises a first PMOS transistor and a first NMOS transistor, wherein said interface circuit comprises a second PMOS transistor and a second NMOS transistor, wherein said first and second PMOS transistors share a p+ source region, and wherein said first and second NMOS transistors share an n+ source region.

17. An integrated circuit comprising:

a semiconductor substrate;

a first drain region disposed in said substrate;

a first channel region disposed in said substrate directly adjacent to said first drain region;

a first gate dielectric overlying said first channel region;

a first gate overlying said first gate dielectric;

a first source region disposed in said substrate directly adjacent to said first channel region;

a second channel region disposed in said substrate directly adjacent to said first source region and on a side of said first source region opposite to said first channel region;

a second gate dielectric overlying said second channel region;

a second gate overlying said second gate dielectric; and

a second drain region disposed in said substrate directly adjacent to said second channel region.

18. The integrated circuit of claim 17, further comprising an input/output pad electrically coupled to said first gate and to said second drain region.

19. The integrated circuit of claim 17, wherein said substrate is p-type, and wherein said source and drain regions are n+ regions.

20. The integrated circuit of claim 17, further comprising an n-well disposed in said substrate around said regions, wherein said substrate is p-type, and wherein said source and drain regions are p+ regions.

21. A method of forming an integrated circuit, said method comprising:

forming a first drain region in a semiconductor substrate;

forming a first source region in said substrate separated from said first drain region solely by a first channel region;

forming a second drain region in said substrate separated from said first source region solely by a second channel region, wherein said second channel region is a different region than said first channel region;

forming a first gate dielectric overlying said first channel region and a second gate dielectric overlying said second channel region; and

forming a first gate overlying said first gate dielectric and a second gate overlying said second gate dielectric.

22. The method of claim 21, further comprising forming an input/output pad on said semiconductor substrate electrically coupled to said first gate and to said second drain region.

23. The method of claim 21, wherein said substrate is p-type, and wherein said source and drain regions are n+ regions.

24. The method of claim 21, further comprising forming said source and drain regions in an n-well in said substrate, wherein said substrate is p-type, and wherein said source and drain regions are p+ regions.